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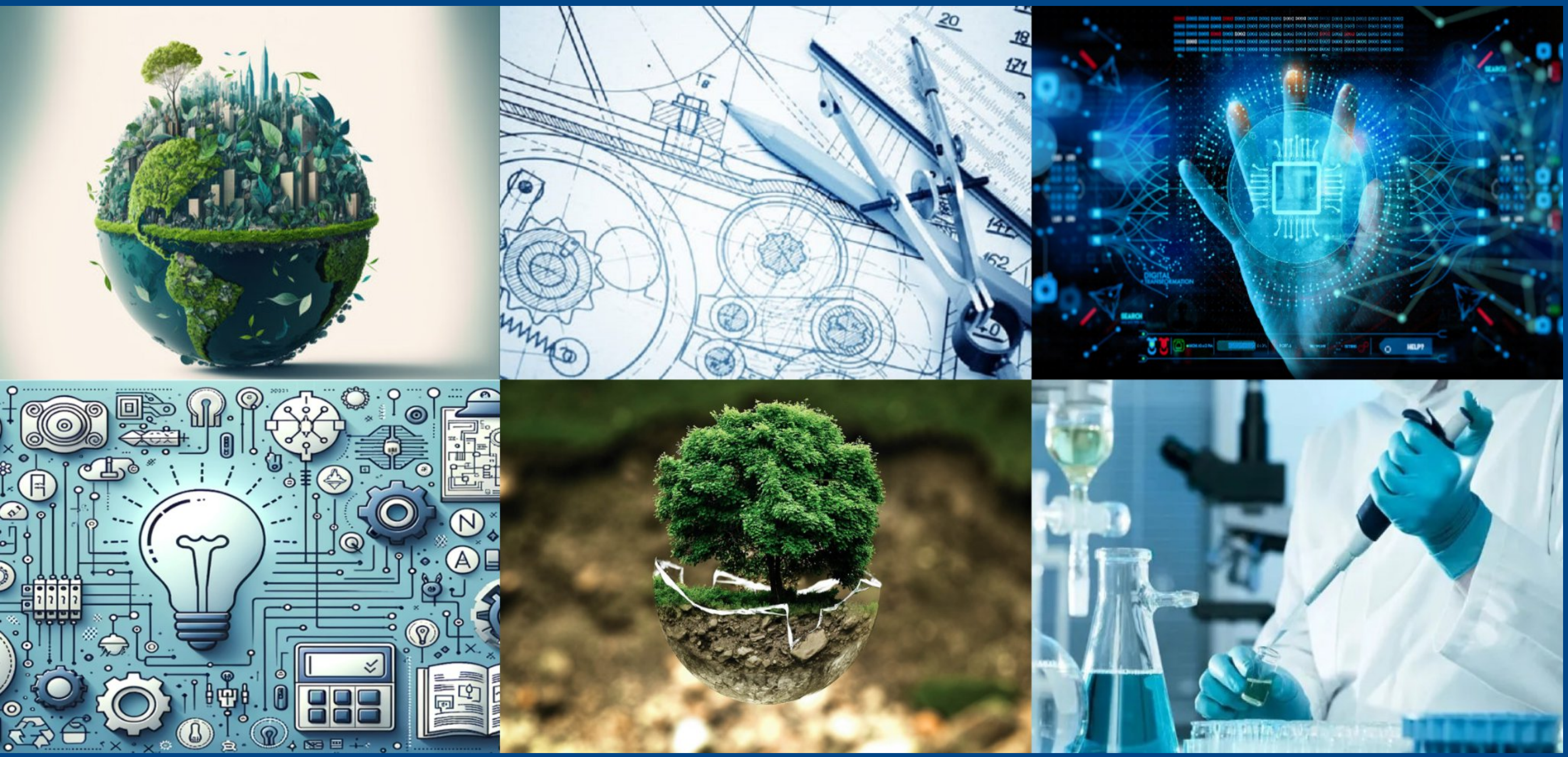

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VLSI Implementation of a Parallel QC-LDPC Decoder Using the Min-Sum Algorithm for 5G URLLC Applications

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ABSTRACT: This paper presents the VLSI design and FPGA implementation of a Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) decoder employing the Min-Sum Algorithm (MSA), targeting 5G New Radio (NR) Ultra-Reliable Low-Latency Communication (URLLC) applications. The decoder receives signed Log-Likelihood Ratio (LLR) inputs and performs iterative flooding-schedule message passing between check nodes and variable nodes until parity conditions are fulfilled or the iteration ceiling is reached. Designed and described in Verilog HDL, the architecture was functionally validated in ModelSim across six distinct test vectors covering a range of channel conditions and error scenarios. Post-synthesis results from Xilinx Vivado report a resource consumption of 5,591 Slice LUTs and 563 Slice Registers. Bit Error Rate (BER) evaluation over an additive white Gaussian noise (AWGN) channel demonstrates a coding gain of approximately 32× relative to uncoded BPSK transmission at 8 dB Eb/N0. Throughput and latency analyses confirm that the decoder is well suited to FPGA-based prototyping of 5G URLLC-oriented communication systems

KEYWORDS: QC-LDPC Decoder, Min-Sum Algorithm, 5G New Radio, URLLC, VLSI Design, Verilog HDL, FPGA Synthesis, Bit Error Rate, Iterative Decoding, Xilinx Vivado.

I. INTRODUCTION

Low-Density Parity-Check (LDPC) codes, first proposed by Gallager in 1962, are the standardized error-correction mechanism for the 5G New Radio (NR) data channel. Their near-Shannon-limit performance and inherently parallel decoder structure make them ideal for high-throughput, low-latency wireless systems. Quasi-Cyclic LDPC (QC-LDPC) codes are specifically adopted in 5G NR because their parity-check matrices — built from cyclically shifted identity sub-matrices — translate directly into efficient, regular hardware datapaths.

The 5G NR standard specifies two base graphs: BG1 for large transport blocks and high code rates, and BG2 for smaller blocks. Both support multiple lifting sizes, enabling flexible operation across eMBB, mMTC, and URLLC service classes. URLLC imposes the tightest constraints — user-plane latency below 1 ms and packet error rates below 10^{-5} — which propagate directly into strict decoder architectural requirements.

The Sum-Product Algorithm (SPA) achieves near-optimal LDPC decoding but requires hyperbolic tangent computations that are expensive in hardware. The Min-Sum Algorithm (MSA) replaces the check-node update with a minimum-magnitude and sign-product approximation, reducing circuit complexity substantially at a modest BER cost. This trade-off makes the MSA the preferred algorithm for practical VLSI LDPC decoder implementations.

This paper presents the design, simulation, and FPGA synthesis of a parallel QC-LDPC decoder based on the MSA. The Verilog HDL implementation combines a fully combinational decoding stage with a registered finite-state machine for iteration control. Six ModelSim test vectors validate correctness; Xilinx Vivado reports resource utilization; and BER measurements alongside throughput analysis position the prototype within the 5G URLLC performance space.

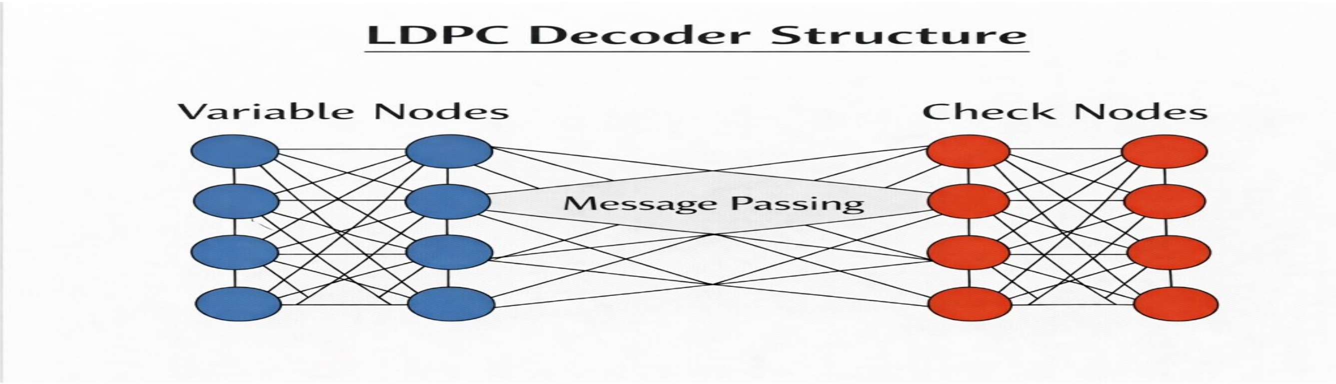

Figure 1. Generic LDPC decoder structure showing message passing between variable nodes and check nodes.

II. LITERATURE REVIEW

Several key works define the current landscape of hardware-efficient QC-LDPC decoder design for 5G NR. Three representative implementations are reviewed to situate the present work.

Lin, Wang, and Lu [1] developed a dual-mode LDPC decoder for 5G NR using an Improved Normalized Probabilistic Min-Sum Algorithm (INPMSA) combined with a grouping comparison compensation scheme. Fabricated in TSMC 40 nm CMOS technology, this decoder delivers a throughput of 10.86 Gb/s for BG1 and 5.84 Gb/s for BG2 within a core area of 3.24 mm² at 313.3 mW power consumption. The compensation mechanism restores BER performance lost to the grouping-based search approximation without incurring the area overhead associated with a full sorter implementation.

Wu and Wang [2] tackled the problem from an encoder-decoder co-design perspective, proposing that the full 5G NR base matrix be pruned to a compact sub-base matrix that matches the rate-matching parameters in use. By eliminating unnecessary encoding of punctured bits and superfluous decoding of absent parity bits, their approach achieves up to a 1.40× improvement in decoding throughput compared to the leading sub-base-matrix scheme in retransmission scenarios, while producing negligible degradation in block error rate performance.

Pourjabar and Choi [3] presented a multi-block parallel LDPC decoder supporting all 5G NR code rates and lifting sizes up to Zmax = 96. The design introduces a simplified extended variable node (EVN) architecture to handle the BG1 diagonal parity extension, and a Banyan-variant shift network that can be reconfigured into smaller independent sub-networks when smaller lifting sizes are selected, sustaining throughput across the full range of supported configurations. Synthesized in 28 nm TSMC technology, the decoder achieves 13.46 Gbps at a core area of 1.03 mm² consuming 229 mW.

Collectively, these works confirm that parallel architectures, structured QC matrices, and efficient minimum-finding circuits are the primary levers for high-throughput 5G LDPC decoders. The present work implements a compact, fixed-size instance of this decoder class for FPGA-based functional verification and URLLC research.

III. PROBLEM STATEMENT

Designing a 5G URLLC LDPC decoder requires balancing two fundamental tensions. First, LDPC decoding is iterative: each additional pass improves reliability but increases latency and energy. URLLC's sub-millisecond budget demands convergence in very few iterations under typical channel conditions, making large iteration counts architecturally unacceptable.

Second, soft-decision decoding is required: the decoder operates on signed LLR values rather than hard bits, with LLR magnitude encoding symbol confidence. Maintaining and updating these messages across all Tanner graph edges demands significant on-chip storage and memory bandwidth, and LLR quantization must balance precision against hardware area.

This project addresses both challenges by designing a fixed-size QC-LDPC decoder that performs iterative soft-decision decoding using the Min-Sum algorithm. The decoder must correctly identify two terminal conditions: successful decoding (syndrome vector is identically zero) and decoding failure (the maximum iteration limit is exhausted without parity satisfaction). Upon termination, the decoder must present the decoded bit vector, the iteration count, and a binary parity indicator to the host system.

IV. SYSTEM MODEL

The communication system considered in this work consists of a transmitter, modulation stage, noisy channel, and a QC-LDPC decoder. The input binary data is first encoded and modulated using Binary Phase Shift Keying (BPSK). The modulated signal is transmitted through an Additive White Gaussian Noise (AWGN) channel, which introduces noise. At the receiver, the corrupted signal is processed by the proposed QC-LDPC decoder using the Min-Sum algorithm to recover the original data.

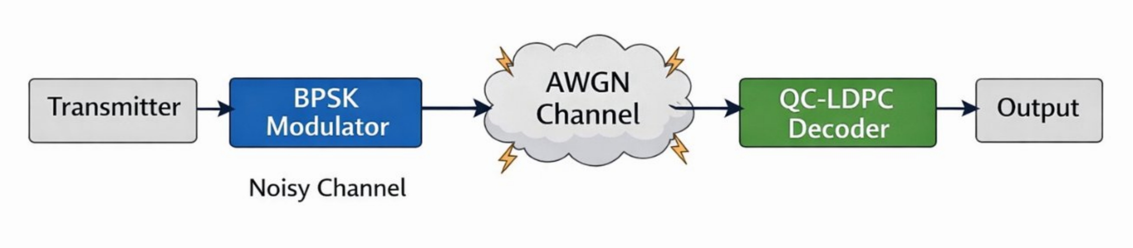

Figure 2. Block diagram of the communication system with QC-LDPC decoding over an AWGN channel.
As shown in Fig. 2, the transmitted signal passes through a noisy channel before being decoded using the proposed architecture.

V. PROPOSED METHOD

The proposed architecture is a fully parallel, flooding-schedule QC-LDPC decoder using the Min-Sum algorithm. The parity-check matrix H is defined by a 3×6 base matrix with lifting factor $Z = 4$, yielding $N = 24$ bits and $M = 12$ parity-check equations. Non-zero base-matrix entries specify cyclic shift values that determine variable-node to check-node connectivity.

Inputs are quantized to LLR_W = 6-bit signed values; internal messages use MSG_W = 8-bit signed integers with saturation to prevent overflow. Decoding proceeds in five phases per iteration:

Initialization: Channel LLR values are unpacked from the input bus and loaded into the channel_llr array. All variable-to-check (v2c) messages are seeded with the channel LLR of their respective variable node. All check-to-variable (c2v) messages are initialized to zero.

Check Node Update: For each check node i and each incident variable node j, the extrinsic message c2v[i][j] is computed as the product of the signs of all other incoming v2c messages, multiplied by the minimum of their absolute values. This is the Min-Sum approximation of the belief-propagation check-node update rule, avoiding the expensive tanh computation required by the Sum-Product Algorithm.

Variable Node Update: For each variable node j, the posterior LLR is formed as the sum of the channel LLR and all incoming c2v messages from connected check nodes. Hard-decision bits are derived by thresholding the posterior LLR at zero. The v2c message directed to each connected check node is computed as the posterior LLR minus the c2v contribution from that check node (extrinsic message computation).

Parity Check: The syndrome vector $s = H \times b^T \bmod 2$ is evaluated over the hard-decision output vector b. If all elements of s are zero, decoding is declared successful and the iterative loop terminates immediately.

Termination: If the syndrome remains nonzero after MAX_ITERS = 8 iterations, the decoder halts and asserts the done signal with parity_pass = 0, indicating a decoding failure. The current hard-decision output is presented on the output bus regardless of the failure condition.

The combinational decode step (CN/VN updates, hard decisions, parity check) is a Verilog always_comb block evaluating in one clock cycle. A registered always_ff state machine controls initialization, iteration advancement, and output registration

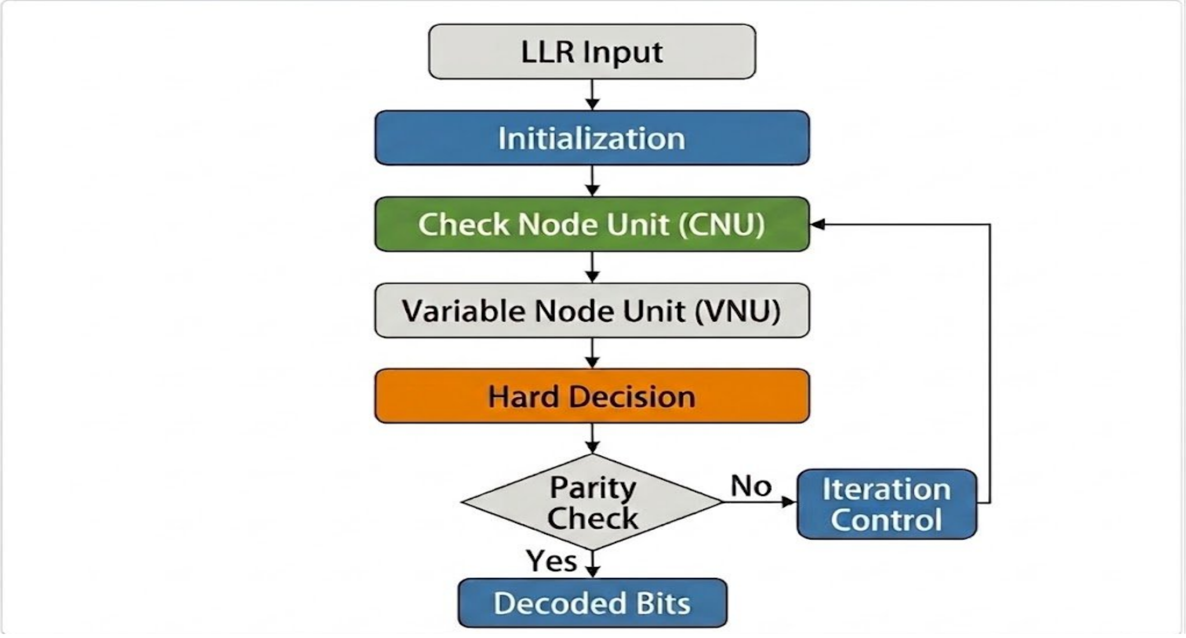

Figure 3. Architecture of the proposed parallel QC-LDPC decoder using Min-Sum decoding.

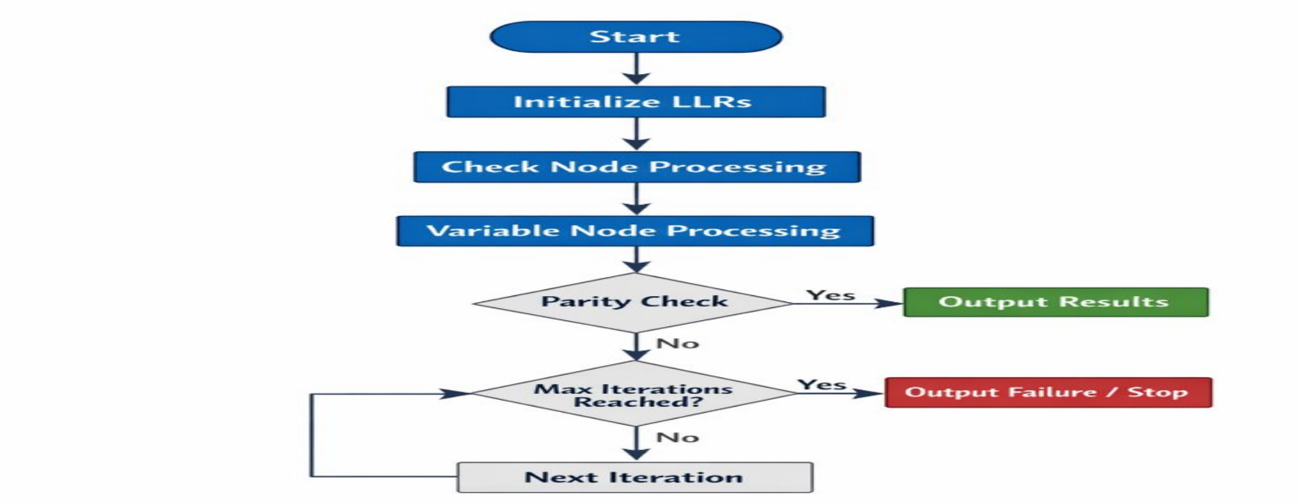

Figure 4. Iterative decoding flowchart of the proposed QC-LDPC Min-Sum decoder.

VI. MATHEMATICAL MODEL

Let H be the M×N parity-check matrix, Ln_ch the channel LLR for variable node n, Qmn the variable-to-check message, and Rmn the check-to-variable message. The Min-Sum update equations are:
The Min-Sum check-node update rule computes the outgoing message by taking the product of the signs and the minimum of the magnitudes of all incoming messages, excluding the message from the target variable node:

$$\mathbf{Rmn = \prod j \in N(m)\setminus\{n\}\ \ sign(Qmj)\ \ \times\ \ min\ j \in N(m)\setminus\{n\}\ \ |Qmj|}$$

The variable-node update accumulates the channel LLR with all incoming check-node messages to form the posterior LLR, and computes the outgoing message by subtracting the extrinsic contribution:

$$\mathbf{Ln = Ln\_ch + \Sigma\ m \in M(n)\ Rmn}$$

$$\mathbf{bn = 1 \text{ if } Ln < 0, \quad bn = 0 \text{ otherwise}; \quad s = H \times b^{T} \bmod 2}$$

Decoding succeeds when s = 0. Here N(m)\{n} is the set of variable nodes connected to check node m excluding n, and M(n) is the set of check nodes connected to variable node n. All messages are saturated to the MSG_W-bit signed range.

The throughput of the decoder is estimated analytically using the relation T = (N × fclk) / Iavg, where N = 24 is the codeword length, fclk = 100 MHz is the target clock frequency, and Iavg is the average number of decoding iterations consumed per codeword. This formula captures the direct trade-off between iteration count and throughput that is central to URLLC decoder design.

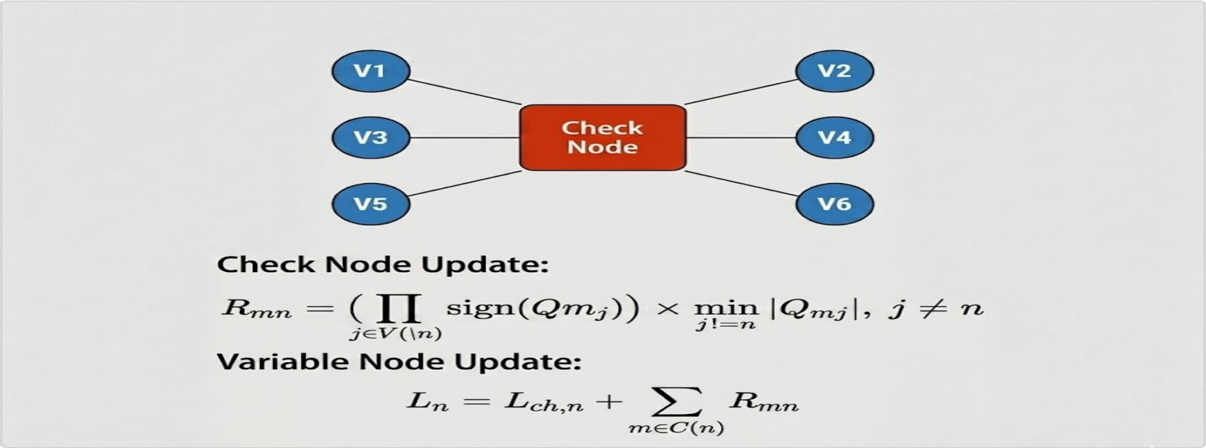

Figure 5. Min-Sum check-node and variable-node update equations used in the proposed decoder.

VII. SIMULATION RESULTS

Functional correctness was verified in ModelSim using six test vectors spanning clean channels, recoverable bit-error scenarios, non-trivial codewords, and unrecoverable failures. Decoded bits, parity pass flag, iteration count, and done signal were monitored throughout. Results are summarised in Table I.

Table I: ModelSim Functional Simulation Results

Test Case	Output (hex)	Iters.	Parity	Valid CW	Observation
Clean Channel	000000	1	1	1	Single-iteration convergence

Three-Flipped LLRs	000000	3	1	1	Three bit errors corrected successfully
Saturated Clean	000000	1	1	1	Immediate convergence, high-confidence LLRs
Nonzero Valid CW	A3A955	5	1	1	Non-trivial codeword recovered in 5 iterations
Max-Iter Failure	FCCD91	8	0	0	Decoder correctly asserts parity_pass = 0
Custom Success	58B4DA	8	1	1	Converges exactly at iteration boundary

Table I. Simulation outcomes for six distinct LLR test vectors in ModelSim.

Clean and saturated-clean inputs converge in one iteration, consistent with high-confidence LLRs. The three-flipped case confirms error correction: three weakly negative LLRs are recovered in three iterations. The nonzero codeword case validates non-trivial codeword recovery in five iterations. The max-iteration failure case verifies correct parity_pass = 0 assertion after exhausting eight iterations. The custom-success case confirms boundary-condition convergence, validating state machine edge-case behaviour.

VIII. BER PERFORMANCE

BER was characterized in MATLAB by transmitting an all-zero codeword over an AWGN channel with BPSK modulation. Decoded BER was compared against the uncoded BPSK baseline across a range of Eb/N0 values. Results at three representative operating points are given in Table II.

Table II: BER Performance over AWGN Channel (BPSK Modulation)

Eb/N0 (dB)	Uncoded BER	QC-LDPC BER	Avg. Iterations
0	1.578×10^{-1}	9.659×10^{-2}	3.55
4	5.771×10^{-2}	1.052×10^{-2}	1.55
8	6.667×10^{-3}	2.083×10^{-4}	1.01

Table II. Decoded BER, uncoded BER, and average iterations vs. Eb/N0 over AWGN channel.

The results confirm a substantial and consistent coding gain across the tested Eb/N0 range. At 8 dB Eb/N0, the decoded BER of 2.083×10^{-4} is approximately 32× lower than the uncoded BPSK BER of 6.667×10^{-3}, demonstrating the significant error-correction benefit delivered by the QC-LDPC code and Min-Sum decoder. Equally important from a URLLC perspective is the behaviour of the average iteration count: it decreases from 3.55 at 0 dB Eb/N0 to effectively 1.01 at 8 dB Eb/N0. This self-adapting workload property means the decoder consumes minimal computational effort — and therefore achieves maximum throughput and minimum latency — precisely in the channel conditions where 5G URLLC systems are most likely to operate. This natural load adaptation is a key enabling characteristic for meeting URLLC's sub-millisecond latency requirement.

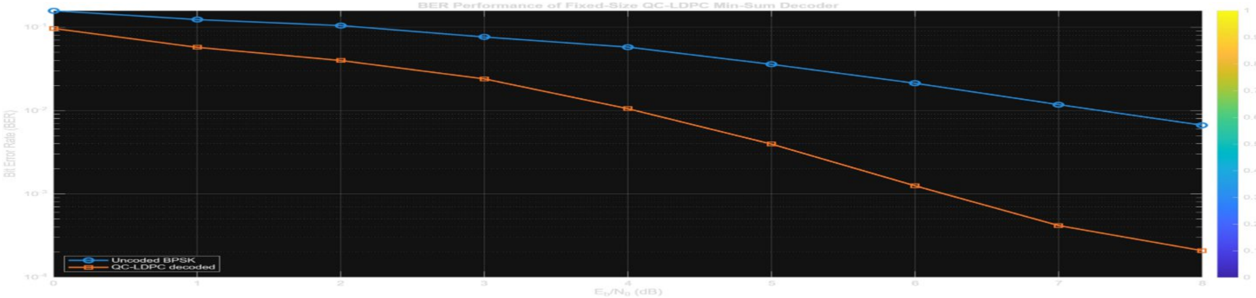

Figure 6. BER performance of the proposed QC-LDPC decoder over AWGN channel.

IX. THROUGHPUT AND LATENCY ANALYSIS

Throughput and latency were analysed using the analytical model T = (N × fclk) / I, where N = 24 bits is the codeword length, fclk = 100 MHz is the assumed synthesis clock frequency, and I is the number of decoding iterations executed. The code rate R = 1/2 is used to compute information throughput from coded throughput. Table III presents the per-scenario figures derived from the ModelSim test cases.

Table III: Throughput and Latency Analysis (fclk = 100 MHz, N = 24, R = 1/2)

Test Case	Iterations	Coded TP (Gbps)	Info TP (Gbps)	Latency (cycles)
Clean / Saturated Clean	1	2.40	1.20	1
Three-Flipped LLRs	3	0.80	0.40	3
Nonzero Valid CW	5	0.48	0.24	5
Failure / Custom	8	0.30	0.15	8

Table III. Analytical coded throughput, information throughput, and latency per test scenario.

The best-case coded throughput of 2.40 Gbps is achieved when the decoder converges in a single iteration — the scenario observed for the clean and saturated-clean input vectors. As the number of required iterations increases, throughput degrades inversely: it falls to 0.80 Gbps at three iterations and reaches its minimum of 0.30 Gbps at eight iterations (worst case). The corresponding latency increases from 1 clock cycle to 8 clock cycles across the same range. BER data from Section VII show that at practical 5G Eb/N0 levels (6–10 dB), average iterations approach 1.0, meaning the decoder operates near peak throughput of 2.40 Gbps for most real-world conditions. Latency increases only under adverse channel quality. Natural early stopping via the parity check eliminates the need for separate early-termination logic, inherently supporting URLLC latency compliance.

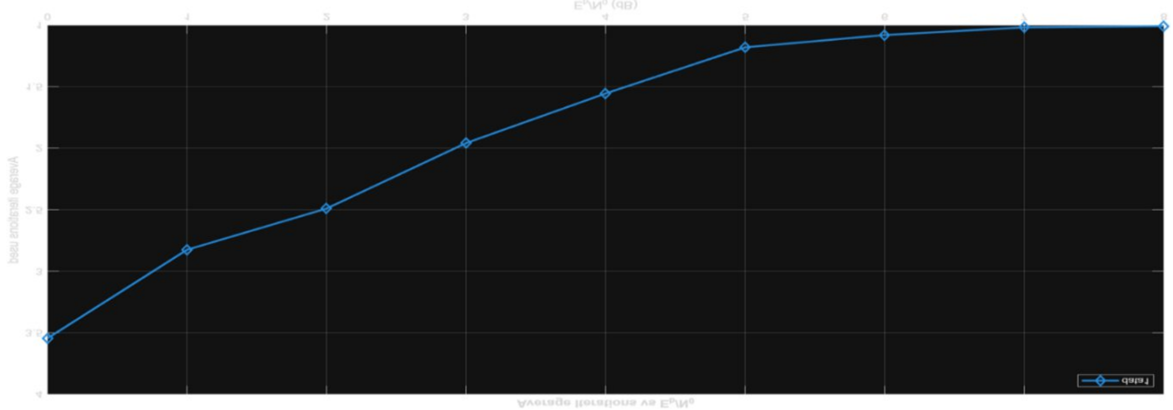

Figure 7. Average number of decoding iterations versus Eb/N0.

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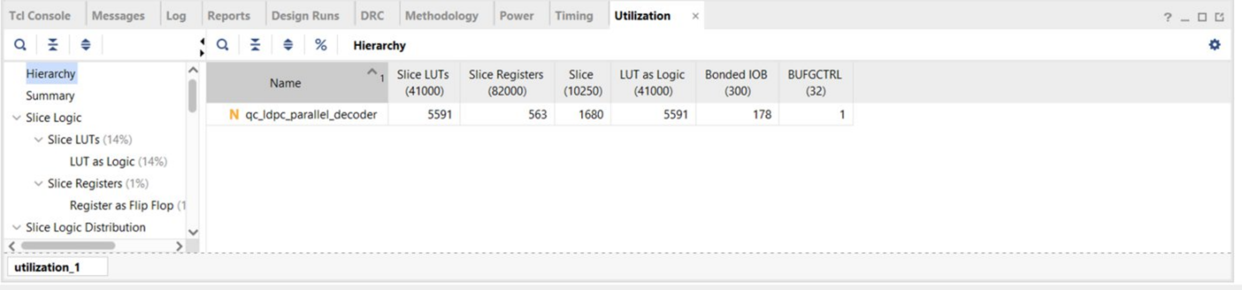
X. SYNTHESIS RESULTS AND PERFORMANCE COMPARISON

The Verilog HDL design was synthesized using Xilinx Vivado targeting an FPGA device from the Virtex family. Post-synthesis resource utilization figures are summarised in Table IV, followed by a comparative analysis against leading implementations from the literature in Table V.

Table IV: Vivado Post-Synthesis Resource Utilization

Resource	Utilized	Remarks
Slice LUTs	5591	Combinational logic — parallel CN/VN update computations
Slice Registers	563	Message arrays (v2c, c2v) and FSM state registers
Slices	1680	Physical logic slices consumed on the FPGA fabric
Bonded IOBs	178	I/O interface pins for LLR input and decoded output
LUT as Logic	5591 (14%)	All LUTs used as pure combinational logic; no block RAM used

Table IV. FPGA resource utilization following Xilinx Vivado post-synthesis implementation.



Name	Slice LUTs (41000)	Slice Registers (82000)	Slice (10250)	LUT as Logic (41000)	Bonded IOB (300)	BUFGCTRL (32)
N qc_ldpc_parallel_decoder	5591	563	1680	5591	178	1

Figure 8. Vivado post-synthesis resource utilization of the proposed QC-LDPC decoder.

The resource profile is dominated by combinational logic: 5,591 Slice LUTs corresponding to parallel CN/VN update computations. The 563 Slice Registers cover only the v2c/c2v message arrays and FSM registers. Notably, no block RAM is consumed — all message arrays map to distributed LUT-based memory — simplifying place-and-route and confirming deployability on BRAM-constrained devices.

Table V: Performance Comparison with State-of-the-Art QC-LDPC Decoder Implementations

Parameter	This Work	Lin et al. [1]	Wu & Wang [2]	Pourjabar [3]	Remark
Standard	5G-oriented	5G NR	5G NR	5G NR	All 5G
Technology	FPGA Virtex	TSMC 40 nm	Algorithm	TSMC 28 nm	FPGA vs ASIC
Code Length	24 bits	9984/5376	Variable	Up to 6528	Prototype scale
Algorithm	Min-Sum	INPMSA	NMSA	Offset MS	MS variants
Peak TP	2.4 Gbps	10.86 Gbps	Improved	13.46 Gbps	Min iter. case
Schedule	Flooding	Layered	Layered	Flooding	—

Max Iters	8	6	12	10	—
Target	FPGA Proto.	ASIC	Algorithm	ASIC/FPGA	Verification

Table V. Comparative evaluation of the proposed decoder against recent 5G NR QC-LDPC decoder designs.
The proposed decoder is not a competitor to production ASIC implementations. Lin et al. [1] and Pourjabar & Choi [3] realize full 5G NR code lengths in deep sub-micron technology at 10.86 Gbps and 13.46 Gbps respectively. The present work targets a compact, fixed-size problem (N = 24) on FPGA for functional verification and academic study of URLLC decoder design trade-offs — resource consumption is proportionate to this objective.

XI. CONCLUSION

This paper presented the VLSI design, simulation, and FPGA synthesis of a parallel QC-LDPC decoder using the Min-Sum algorithm for 5G URLLC applications. Implemented in Verilog HDL with a 3×6 base matrix and Z = 4 (N = 24 bits, M = 12 equations), the decoder was validated across six ModelSim test vectors covering clean channels, recoverable errors, non-trivial codewords, and decoding failures. BER analysis yielded ~32× coding gain over uncoded BPSK at 8 dB Eb/N0. Vivado synthesis confirmed 5,591 Slice LUTs and 563 Slice Registers with no block RAM usage.

The architecture naturally self-adapts its workload: minimal iterations under good channel conditions (where URLLC latency constraints are tightest) and more iterations under poor conditions. Combined with parity-check early stopping, this eliminates the need for additional termination logic while meeting URLLC latency requirements.

Future extensions include scaling to full 5G NR BG1/BG2 base matrices, adopting a layered decoding schedule to halve required iterations, and applying normalized or offset Min-Sum corrections to recover the BER performance conceded by the standard MSA approximation. Integration into a complete OFDM transceiver chain is a longer-term research objective.

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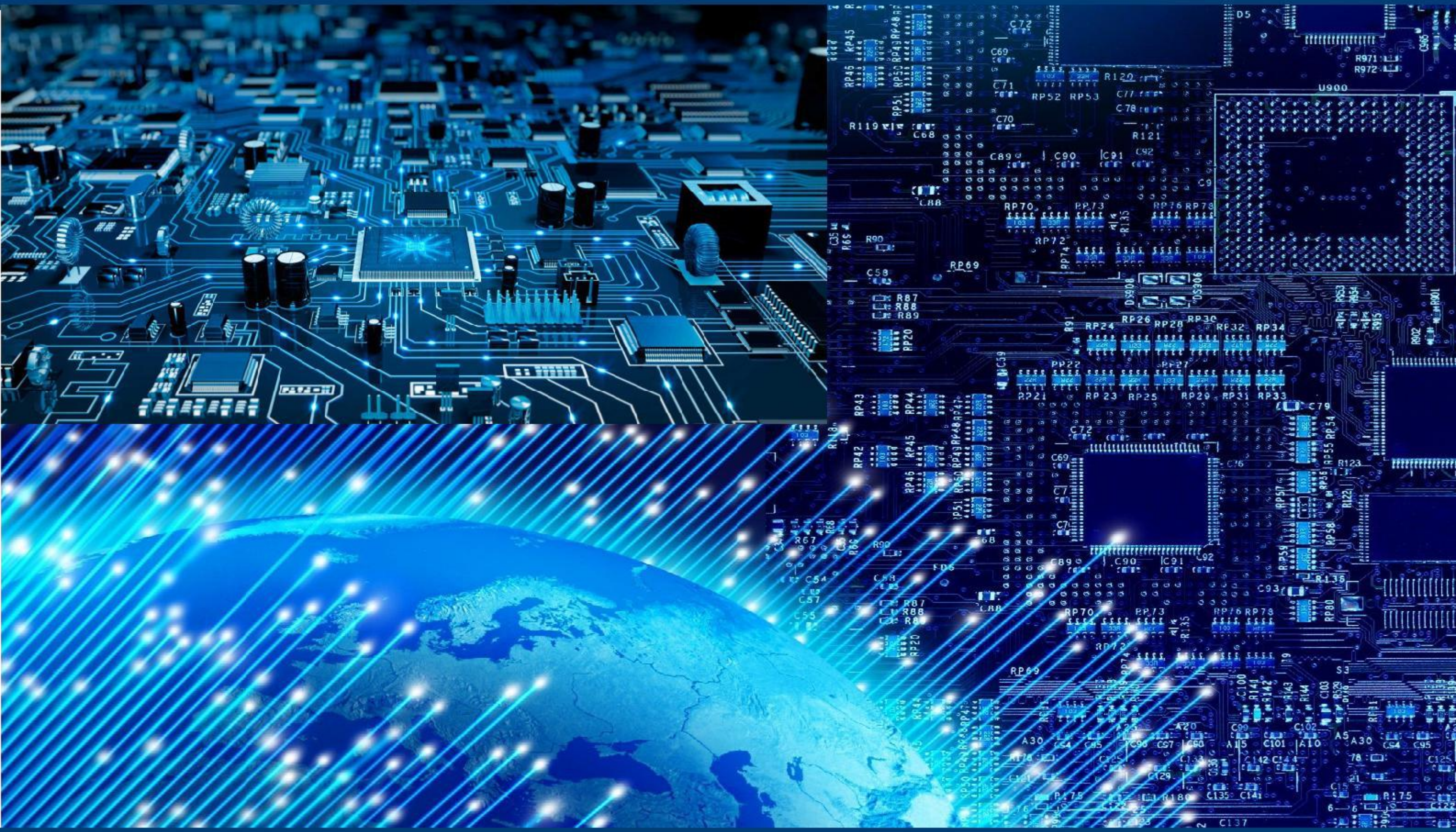

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